What is Claimed is:

[c1] A read only memory (ROM) cell connected to a true bitline and a complement bitline, said ROM cell comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline.

[c2] The ROM cell in claim 1, wherein said first transistor further comprises a first source, and said second transistor further comprises a second source, and

wherein a connection of one of said first source and said second source to a ground programs said ROM cell

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[c3] The ROM cell in claim 2, wherein only one of said first source and said second source is connected to said ground and the other of said first source and said second source is insulated from electrical connections.

[c4] The ROM cell in claim 2, wherein said connection comprises an electrical connection formed during manufacturing of said first transistor and said second transistor.

[c5] The ROM cell in claim 1, wherein said first transistor further comprises a first gate connected to a wordline and said second transistor further comprises a second gate connected to said wordline.

[c6] The ROM cell in claim 1, wherein said second transistor comprises a complement transistor to said first transistor.

[c7] The ROM cell in claim 1, wherein said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell in said array.

[c8] A read only memory (ROM) cell array connected to a true bitline and a complement bitline, each ROM cell in said ROM cell array comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline.

[c9] The ROM cell array in claim 8, wherein said first transistor further comprises a first source, and said second transistor further comprises a second source, and wherein a connection of one of said first source and said second source to a ground programs said ROM cell.

[c10] The ROM cell array in claim 9, wherein only one of said first source and said second source is connected to said ground and the other of said first source and said second source is insulated from electrical connections.

[c11] The ROM cell array in claim 9, wherein said connection comprises an electrical connection formed during manufacturing of said first transistor and said second transistor.

[c12] The ROM cell array in claim 8, wherein said first transistor further comprises a first gate connected to a wordline and said second transistor further comprises a second gate connected to said wordline.

[c13] The ROM cell array in claim 8, wherein said second transistor comprises a complement transistor to said first transistor.

[c14] The ROM cell array in claim 8, wherein said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell in said array.

[c15] A method of forming a read only memory (ROM) cell, said method comprising:

forming a first drain of a first transistor such that said first drain is connected to a true bitline;

forming a second drain of a second transistor such that said second drain is connected to a complement bitline; and

forming a first source of said first transistor and a second source of said second transistor such that one of said first source and said second source is connected to ground.

[c16] The method in claim 15, wherein a connection of one of said first source and

said second source to said ground programs said ROM cell.

[c17] The method in claim 15, wherein said forming of said first source and said second source only connects one of said first source and said second source to said ground and insulates the other of said first source and said second source from electrical connections.

[c18] The method in claim 15, further comprising:

forming a first gate of said first transistor connected to a wordline; and

forming a second gate of said second transistor connected to said wordline.

[c19] The method in claim 15, wherein said second transistor comprises a complement transistor to said first transistor.

[c20] The method in claim 15, wherein said forming of said first drain and said second drain is performed such that said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell.

[c21] A read only memory (ROM) cell connected to a true bitline and a complement bitline, said ROM cell comprising:

a first transistor having a first drain and a first source; and

a second transistor having a second drain and a second source,

wherein said first source and said second source are connected to ground, and

wherein a connection of one of said first drain to said true bitline and said second drain to said complement bitline programs said ROM cell.

[c22] The ROM cell in claim 21, wherein only one of said first drain and said second drain is connected to one of said true bitline and said complement bitline, and the other of said first drain and said second drain is insulated from electrical connections.

[c23] The ROM cell in claim 21, wherein said connection comprises an electrical connection formed during manufacturing of said first transistor and said second transistor.

[c24] The ROM cell in claim 21, wherein said first transistor further comprises a first gate connected to a wordline and said second transistor further comprises a second gate connected to said wordline.

[c25] The ROM cell in claim 21, wherein said second transistor comprises a complement transistor to said first transistor.

[c26] The ROM cell in claim 21, wherein said ROM cell shares said first source and said second source with corresponding sources of adjacent ROM cells.